

(a) Forward bias state: The device is shown with a negative terminal (-) on the left and a positive terminal (+) on the right. An arrow labeled "LIGHT" points upwards from the center. The internal structure includes layers 11, 12, 131, 132, 14, 15, and 16. Charge carriers are shown as electrons (e-) moving from the left and holes (h+) moving from the right towards the center.

(b) Reverse bias state: The device is shown with a positive terminal (+) on the left and a negative terminal (-) on the right. An arrow labeled "LIGHT" points upwards from the center. The internal structure is the same as in (a). Charge carriers are shown as electrons (e-) moving from the left and holes (h+) moving from the right towards the center.

A cross-sectional view of a semiconductor device. It shows a substrate 21 with a thin layer 22 on top. Two electrodes, 23 and 25, are formed on the surface. Electrode 23 is connected to a positive terminal (+) and electrode 25 to a negative terminal (-). A layer 24 is formed over the electrodes and substrate. A layer 26 is formed on top of layer 24. The device is shown in a cross-section with various layers and electrodes labeled with numbers and signs.

Figure 1 consists of six cross-sectional views of a semiconductor device, labeled (a) through (f), illustrating the sequential steps of its fabrication:

- (a)** Shows a substrate (21) with a first conductive layer (22) deposited on its top surface.
- (b)** Shows the formation of a second conductive layer (271) on top of the first conductive layer (22). The second conductive layer (271) is patterned to form a raised portion (281).
- (c)** Shows the formation of a third conductive layer (24) on top of the second conductive layer (271). The third conductive layer (24) is patterned to form a raised portion (23).
- (d)** Shows the formation of a fourth conductive layer (282) on top of the third conductive layer (24). The fourth conductive layer (282) is patterned to form a raised portion (272).
- (e)** Shows the formation of a fifth conductive layer (25) on top of the fourth conductive layer (282). The fifth conductive layer (25) is patterned to form a raised portion (272).
- (f)** Shows the final device structure with the fifth conductive layer (25) and the raised portion (272) on top of the fourth conductive layer (282).

Fig. 4

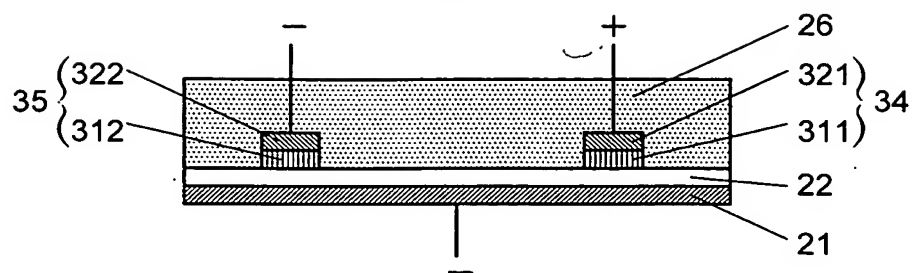


Fig. 5

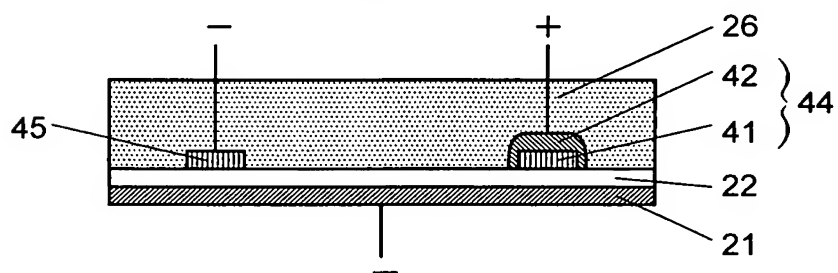


Fig. 6

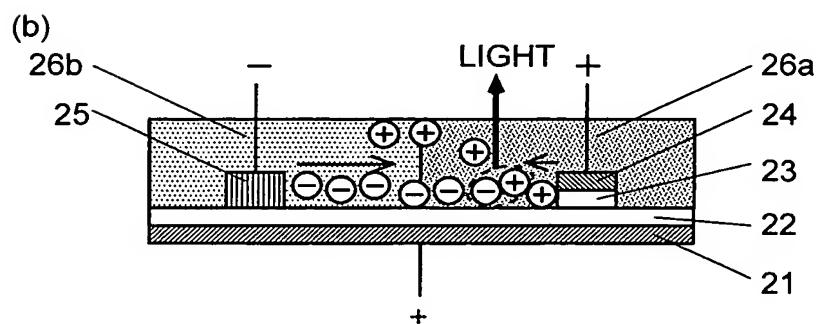
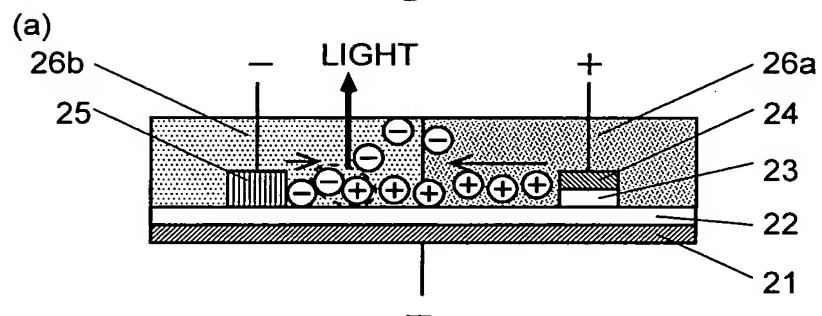


Fig. 7

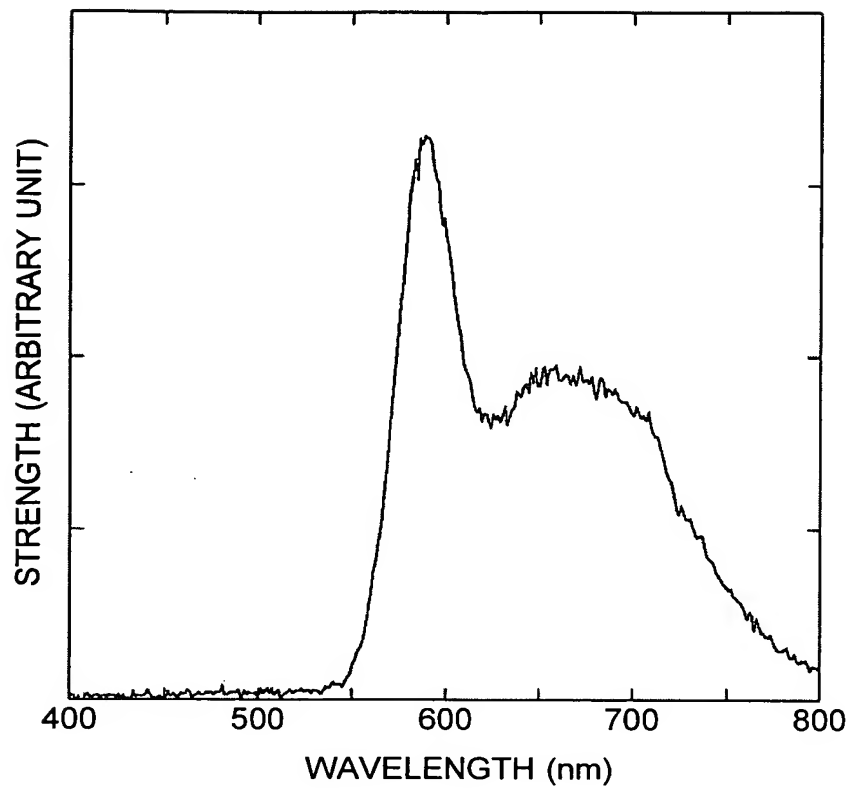


Fig. 8

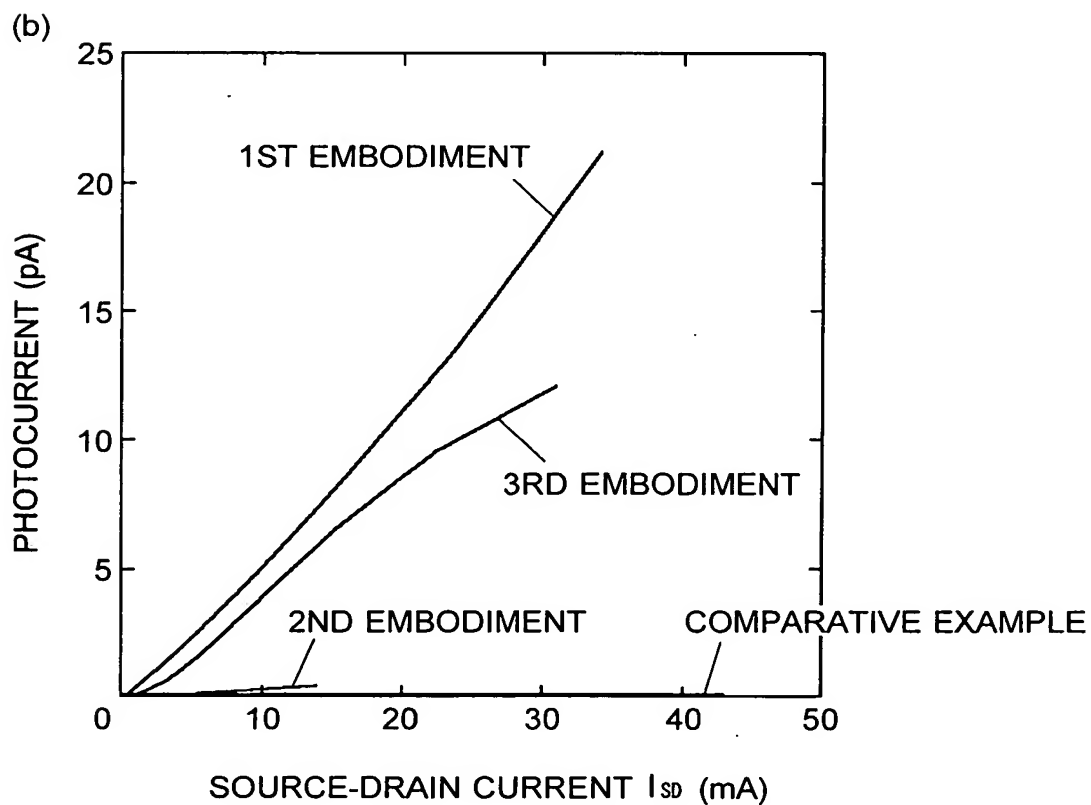
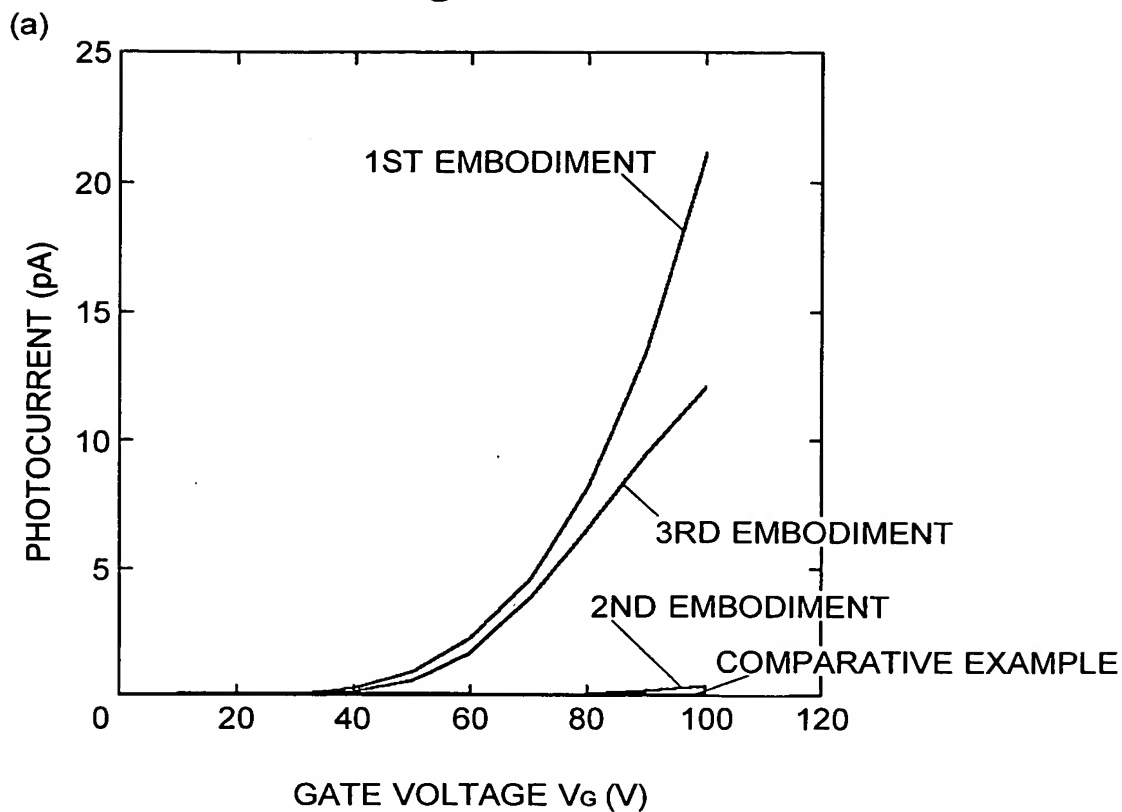


Fig. 9

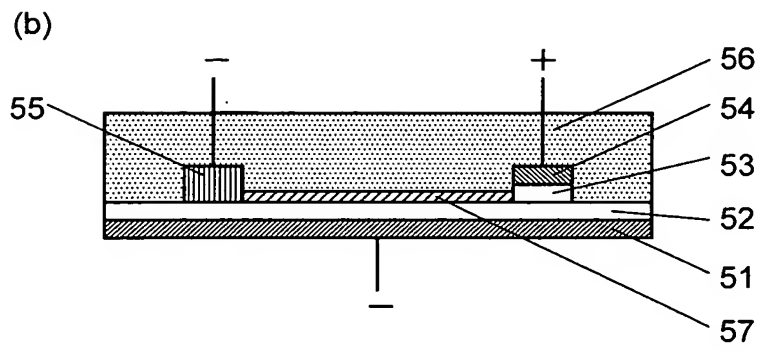
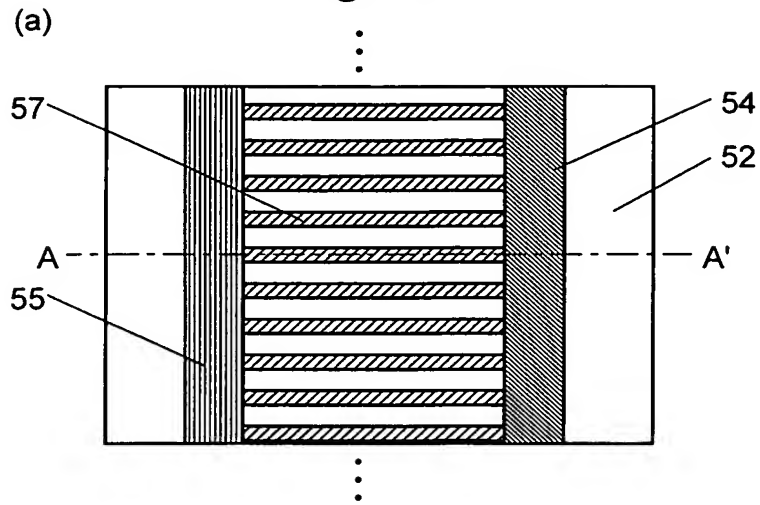


Fig. 10

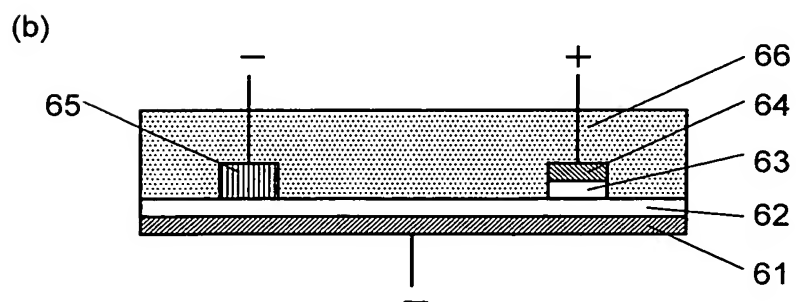
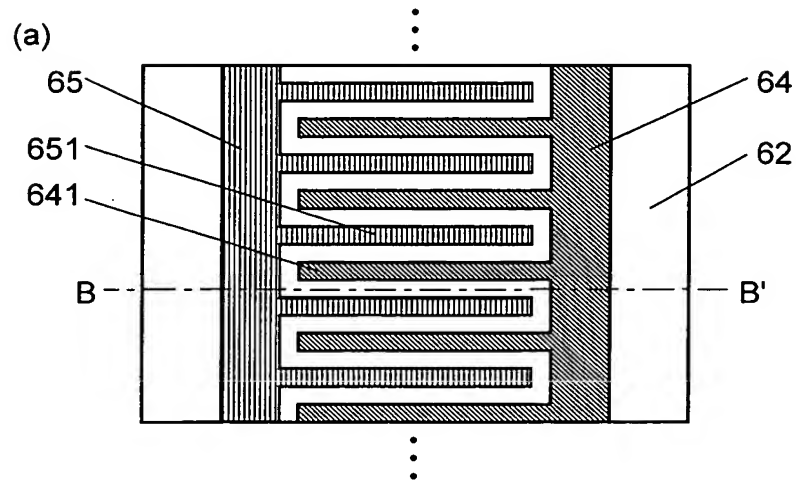


Fig. 11

